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EXAMINER	
NATNAEL, PAULOS M	
ART UNIT	**PAPER NUMBER**
2614	19

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/191,629	TRAN ET AL.	
	Examiner	Art Unit	
	Paulos M. Natnael	2614	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6,8-18,20-38, 40-46,48-52* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *44,45 and 48-52* is/are allowed.

6)☒ Claim(s) *1-4,6,8-18,20-38,40-43 and 46* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims **40-43,46** are rejected under 35 U.S.C. 102(e) as being anticipated by Dye, U.S. Patent No. **6,067,098**.

Considering claim **40**, Dye discloses the following claimed subject matter, note;

a) a central processing unit (CPU), is met by CPU 102 (FIG.2A).

b) the claimed local bus coupled to the CPU, is met by PCI/USB, Fig. 2A/2B, which, given reasonably broad interpretation, is coupled to the CPU through 140.

c) the claimed graphics controller coupled to the local bus, is met by IMC 140, Fig. 2A+ which comprises a graphics engine 210 as illustrated in fig.6.

d) the claimed display device for receiving outgoing digital television data from the graphics controller is met by display 142, Fig. 2A;

e) the claimed digital television/local bus interface logic coupled to the local bus for storing incoming digital television data and the outgoing digital television data and selectively providing the outgoing digital television data over the local bus to the graphics controller when a programmed position of the display device is refreshed, is met by Interactive Media Controller 140 and System Memory 110, Fig. 2A;

Considering claim **41**, the claimed core logic coupled between the local bus and the graphics controller is met by Bus I/F logic 202, figs. 5 and 6;

Considering claim **42**, the claimed digital television decoder for providing incoming television data to the digital television/local bus interface logic is met by decoder 172, Fig.3;

Considering claim **43**, the claimed digital television tuner for providing incoming digital television data to the digital television decoder, is inherent in televisions system such as Dye's (see the television system Fig.1B);

Considering claim **46**, the claimed wherein the local bus comprises a peripheral component interconnect (PCI) bus, is met by PCI (fig.2A).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims **1-4,6, 8-18, 20-38** are rejected under 35 U.S.C. 103(a) as being unpatentable over Dye, U.S. Patent No. **6,067,098**.

Considering claim **1**, Dye discloses the following claimed subject matter, note;

c) the claimed method of monitoring refresh of a display device coupled to the system is met by the CPU 102, fig.3.

d) the claimed method of transmitting the outgoing frames of digital television data in the second frame buffer to a graphics controller to be displayed on a display device when a programmed position of the display device is refreshed is met by the Display Refresh List (VDRL) Engine 240, which is part of the integrated memory controller (IMC) 140 Fig.3, and that "executes the video display refresh list". (col. 21, lines 22-25).

Except for;

a) the claimed method of storing incoming frames of digital television data in a first frame buffer,of an interface logic;

b) the claimed method of reading outgoing digital television data from a second frame buffer, of an interface logic;

Regarding (a) and (b), Dye discloses that "The IMC 140 uses techniques to improve overall system performance and user response time by use of the main system memory as a virtual graphical frame buffer and program/data storage. The IMC 140 provides a unique system level architecture that reduces data bandwidth requirements for general media input/output functions. Because the host CPU 102 is not required to move data between main memory and the graphics and audio and telephony subsystems as in conventional computers, data can reside virtually in the same subsystem as the main memory. Therefore, for media output data (audio, video, telephony) the host CPU or DMA master is not limited by external available proprietary bus bandwidth, thus improving overall system throughput." (Col. 11, lines 52-65)

Therefore, it would have been obvious to the skilled in the art at the time the invention was made to implement the system of Dye by utilizing the system memory for both incoming and outgoing frames of television signals instead of using separate frame buffers for storing incoming data and for storing outgoing data, so that the system as whole is made more compact and less costly.

Considering claim **2,** Dye discloses the following claimed subject matter, note;

a) storing the incoming frames of digital television data in the second frame buffer
b) reading the outgoing frames of digital television data from the first frame buffer
c) transmitting the outgoing frames of digital television data in the first frame buffer to the display device when the programmed position of the display device is refreshed.

Regarding claim 2, see rejection of claim 1(a),(b) and (d), respectively.

Considering claim **3,** the claimed method of detecting whether the outgoing frames of digital television data is stored in the first frame buffer or the second frame buffer, is met by the CPU 102, fig.3;

Considering claim **4**, the claimed method of monitoring step comprising the step of monitoring a horizontal sync and a vertical sync of the display device, is met by the disclosure "The IMC 140 couples to a display device 142, such as a computer video monitor or television screen, among others. The IMC 140 generates appropriate video signals for driving display device 142. The IMC 140 preferably generates red, green, blue (RGB) signals as well as vertical and horizontal synchronization signals for generating images on the display 142. The IMC 140 also generates NTSC video signals, PAL video signals, or video signals for other analog or digital television/video formats. The IMC 140 may generate any of various types of signals for controlling a display device or video monitor. As shown, the IMC 140 preferably uses a serial control bus, such as the I2C serial bus, for control of the display device 142." (col. 10, lines 46-58)

Considering claim **6**, Dye discloses all claimed subject matter, except for;

The claimed method of transmitting the outgoing frames of digital television data over a peripheral component interconnect (PCI) bus, is met by PCI/USB busses, Fig.2A and 2B.

Considering claim **8**, Dye discloses the following claimed subject matter, note;

a) a central processing unit (CPU), is met by CPU 102 (fig.2A).

b) a graphics controller coupled to the CPU, is met by IMC 140 which comprises graphics engine 212 illustrated in fig.6;

c) the claimed local bus coupled to the CPU and graphsics controller is met by PCI/USB Fig.2A;

d) the claimed Digital television interface for receiving incoming digital TV data, is met by Decoder 172, fig. 3;

e) a local bus interface for transmitting outgoing digital television data to the graphics controller over the local bus is met by I^2C bus system, fig.6;

f) the claimed memory controller for storing the incoming digital television data to one frame buffer and reading the outgoing digital television data from another frame buffer; digital television interface for receiving incoming digital television data, is met by Memory controllers 221 and 222, fig. 6;

Except for;

g) a first frame buffer for storing the incoming digital television data and the outgoing digital television data in an alternating manner;

h) second frame buffer for storing the outgoing digital television data and the incoming digital television data in an alternating manner;

Regarding g) and h), see rejection of claim 1 (a) and (b).

Considering claim **9**, see rejection of claim 6.

Considering claim **10**, the claimed display device coupled to the local bus for receiving outgoing digital television data over the local bus is met by display 142, figs. 2A-2B.

Considering claim **11,** the claimed wherein the memory controller stores the incoming digital television data to the first frame buffer and reads the outgoing digital television data from the second frame buffer on a first portion of a refresh of a display device and transmits the outgoing digital television data in the second frame buffer to the display device on a second portion of the refresh of the display device is met by memory controllers 221 and 222, fig.6;

Considering claim **12**, the claimed wherein the memory controller stores the incoming digital television data to the *second frame buffer* and reads the outgoing digital television data from the first frame buffer on a first portion of a refresh of a display

device and transmits the outgoing digital television data in the first frame buffer to the display device on a second portion of the refresh of the display device;

Regarding claim 12, see rejection of claim 1 (a) and (b).

Considering claim **13**, the claimed wherein the local bus interface monitors a refresh of display device for receiving the outgoing digital television data is met by CPU 102, fig.2;

Considering claim **14**, the claimed wherein a refresh rate of the incoming digital television data is decoupled from a refresh rate of the outgoing digital television data.

Regarding 14, see rejection of claim 1(d).

Considering claim **15**, the digital television local bus logic further comprising: a write state machine for detecting whether the incoming digital television data is being written to the first frame buffer or the second frame buffer, is met by the disclosure that "The high level graphical protocol used by the IMC 140 of the present invention eliminates many of the CPU reads and writes of graphical information that are required in prior art systems. Instead, a system incorporating an IMC 140 according to the present invention includes a high level graphical protocol whereby the CPU 102 instructs the IMC 140 to manipulate the data stored in the system memory 110...Rather, the IMC 140 reads the text data into the system memory 110, preferably in ASCII format, and the IMC 140 processes the text data for display output. This operation is performed under the direction of the CPU 102 through the high level graphical protocol used by the IMC 140...In current prior art systems, this operation requires either extra cost for memory in the graphical subsystem, i.e., additional video memory or VRAM, or the CPU

102 is required to move the occluded information from the graphical subsystem back into the system memory for temporary storage." (col. 13, lines 29-60)

Considering claim **16**, the claimed the digital television/local bus logic further comprising: a read state machine for informing the memory controller of a frame buffer from which to read the outgoing digital television data.

Regarding claim 16, see rejection of claim 15.

Considering claim **17**, a digital television/local bus interface logic, comprising:
a) the claimed a digital television interface for receiving incoming digital television data is met by the Host I/F 202, Fig.6;
b) the claimed a local bus interface for transmitting outgoing digital television data to the graphics controller for display on a display device is met by PCI or USB, Fig. 2A;

e) the claimed a memory controller for storing the incoming digital television data to one frame buffer and reading the outgoing digital television data from another frame buffer on a first portion of a refresh of a display device and transmitting the outgoing digital television data in the one frame buffer to the display device on a second portion of the refresh of the display device is met by the Memory controllers 221 and 222, fig. 6;

Except for;
c) the claimed a first frame buffer for storing the incoming digital television data and the outgoing digital television data in an alternating manner;
d) the claimed a second frame buffer for storing the outgoing digital television data and the incoming digital television data in an alternating manner;

Regarding c) and d), see rejection of claim 1 (a) and (b).

Considering claim **18**, the claimed wherein the local bus interface comprises a peripheral component interconnect (PCI) interface is met by PCI, fig.2A.

Considering claim **20,** see rejection of claim 11.
Considering claim **21,** see rejection of claim 12.
Considering claim **22,** see rejection of claim 14.
Considering claim **23,** see rejection of claim 15.
Considering claim **24,** see rejection of claim 16.

Considering claim **25,** Dye discloses the following claimed subject matter, note;
a) the claimed a first interface means for receiving incoming frames of digital television data is met by Host I/F 202, fig. 6;

b)a second interface means for transmitting outgoing frames of digital television data by the 194/CCIR656 video in/out, fig. 3;

e) the claimed means for storing the incoming digital television data to one means for storing and reading the outgoing frames of digital television data from another buffer means is met by CPU 102, fig.3;

except for;

c) the claimed first means for storing the incoming frames of digital television data and the outgoing digital television data in an alternating manner;

d) a second means for storing the outgoing frames of digital television data and the incoming digital television data in an alternating manner;

Regarding c) and d), see rejection of claim 1 (a) and (b).

Considering claim **26**, the claimed wherein the means for transmitting the outgoing frames of digital television data comprises a peripheral component interconnect (PCI) interface.

Regarding claim 26, see rejection of claim 6.

Considering claim **27**, the claimed the means for transmitting the outgoing frames of digital television data transmits the outgoing frames of digital television data over a local bus is met by HD_bus 207, fig.6;

Considering claim **28**, see rejection of claim 15.

Considering claim **29**, see rejection of claim 16.

Considering claim **30**, the claimed wherein the first interface means for receiving the incoming digital television data comprises a digital television interface.

Regarding claim 30, see rejection of claim 25 (a) and (b).

Considering claim **31**, see rejection of claim 11.

Considering claim **32**, see rejection of claim 12.

Considering claim **33**, see rejection of claim 14.

Considering claim **34**, Dye discloses the following claimed subject matter, note;

c) the claimed a means for monitoring refresh of a display device is met by CPU 102, fig. 3;

d) the claimed a means for transmitting the outgoing digital television data in one of the means for storing to a means for controlling graphics for display on a display device when a programmed position of the display device is refreshed, is met by Storage FIFO 244, fig.6;

Except for;

a) the claimed storing means for storing the incoming digital television data and the outgoing digital television data in an alternating manner;

b) a second means for storing the outgoing digital television data and the incoming digital television data in an alternating manner;

Regarding a) and b), see rejection of claim 1(a) and (b).

Considering claim **35**, a means for reading the outgoing digital television data from a storing means is met by display storage FIFO 244, fig.6; (see also rejection of claim 1 (a) and (b))

Considering claim **36**, the claimed means for monitoring a horizontal sync and a vertical sync of the display device is met by the disclosure "The IMC 140 preferably generates red, green, blue (RGB) signals as well as vertical and horizontal synchronization signals for generating images on the display 142." (col. 10, lines 49-52)

Considering claim **37**, the claimed a means for detecting whether the outgoing digital television data is stored in the first means for storing or the second for storing, is met by CPU 102, FIG.3; (see col. 13, lines 29-60 and rejection of claim 34(a) and (b))

Considering claim **38**, see rejection of claim 6.

Response to Arguments

Applicant's Arguments

1) Dye fails to teach or render obvious all the limitations of claim 1. The disclosure of Dye appears to be directed to avoiding the relocation of large portions of video data by transferring, in its stead, display refresh lists...

2) Concerning claim 8: If Dye's integrated memory controller 140 is the claimed interface logic, then Dye fails to teach or fairly suggest transmitting the outgoing frames of digital television data to a graphics controller to be displayed on a display device. On the other hand, if Dye's integrated memory controller 140 is the claimed graphics controller, the Dye fails to teach or fairly suggest the storing and reading to frame buffers in the interface logic.

3) Concerning Claim 17: While dye may disclose both a PCI and a USB bus, Dye fails to teach or fairly suggest that the outgoing digital television data should be transferred to a graphics controller over either of these busses.

4) Concerning Claim 25: Dye fails to teach or render obvious all the limitations of claim 25.

5) Concerning claim 34: Dye fails to teach or render obvious all the limitations of claim 34;

6) Claim 40 specifically recites a CPU... If Dye's CPU 102 is the claimed graphics controller....

Examiner's Response

1) Dye discloses a video/graphics control which performs pointer-based display list video refresh operation. In Fig.2A, Dye discloses a system which includes the Interactive media controller 140, busses PCI and USB, Video input/output which uses I^2C bus, system memory 110, and display 142. The detailed circuitry of the Controller 140 is shown in Figs. 5 and 6. As can be seen from Fig.6, a local bus, HD_bus, is coupled to the data Fifo 205 and another bus, Dbus2, couples the HD_bus to the fifo 205 with memory controllers 221/22 and other components of the controller (IMC 140). And whether Dye calls the HD_bus local bus or not, the function of HD_bus is, as can be seen from Fig.6 which is part of the disclosure of the Dye reference, the bus is a local bus.

Furthermore, Dye teaches a television system which includes the IMC system and method of the present invention. In FIG. 1B, the television system 53 includes a display screen 59. The television system also preferably includes a set top box 57 which couples through a cable, such as a fiber optic cable or coaxial cable, for receiving video images for display on the television screen 59. The IMC of the present invention may be comprised in the television system unit 53 and/or may be comprised in the set top box 57. In other words, the IMC may be comprised in the set top box 57, or the IMC of the present invention may be integrated into the television, wherein the set top box 57 is optionally not included. The television system 53 is preferably a digital television. Alternatively, the television 53 is an analog television, wherein the set top box 57 operates to receive and/or store digital video data and provide analog video signals to the analog television. The television system 53 may also be adapted for interactive television or Internet applications, e.g., WebTV. In this case, the set top box includes a

return path, such as a POTS telephone, ISDN, or DSL connection, for return data." (col. 8, lines 14-35)

Therefore, the argument that the disclosure of Dye appears to be directed to avoiding the relocation of large portions of video data by transferring, in its stead, display refresh lists, is unpersuasive, giving the teaching of Dye as shown above.

2) Concerning the newly amended claim 8, please see rejection of claim 8;

3) Dye discloses, not only PCI and USB busses, but also discloses I^2C bus to connect IMC 140 to the video decoder 172, which is an MPEG decoder.

4) Examiner agrees that Dye doesn't specifically disclose some of the limitations. Examiner nevertheless rejected claim 25 under ***35 USC § 103*** rejection, not under 35 U.S.C. 102 and, therefore, examiner could not assert all limitations of claim 25 were met.

5) Again, Examiner agrees that Dye doesn't specifically disclose all of the limitations in claim 34. Examiner nevertheless rejected claim 34 under ***35 USC § 103*** rejection, not under 35 U.S.C. 102 and, therefore, examiner could not assert all limitations of claim 34 were met. See rejection of claim 34.

6) As for the newly amended claims 40, see rejection of claim 40 above.

Allowable Subject Matter

5. Claims **44, 45, 48-52** remain allowable over the cited prior art.

6. The following is a statement of reasons for the indication of allowable subject matter: the prior art fails to disclose a method for transferring digital television data in a system having a first frame buffer and a second frame buffer comprising: wherein the graphics controller provides a feedback signal to the digital television/local bus interface logic to indicate whether the programmed position of the display device is refreshed, as in claim **44**; and wherein the feedback signal comprises a horizontal sync and a vertical sync of the display device, as in claim **45**;

A memory controller for storing the first incoming digital television data stream to the first frame buffer or the second frame buffer and reading the first outgoing digital television data stream from the second frame buffer or the first frame buffer on a first portion of a refresh of a display device, storing the second incoming digital television data stream to the third frame buffer or the fourth frame buffer and reading the second outgoing digital television data stream from the fourth frame buffer or the third frame buffer on the first portion of the refresh of the display device, transmitting the first outgoing digital television data stream to the display device on a second portion of the refresh of the display device, and transmitting the second outgoing digital television data stream to the display device on the second portion of the refresh of the display device, as in claim **48**.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paulos M. Natnael whose telephone number is (703) 305-0019. The examiner can normally be reached on 9:00am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Miller can be reached on (703) 305-4795. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PMN
May 15, 2004